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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. EN997064

#22

In Re Application Of: **K. Covert et al**

Serial No.	Filing Date	Examiner	Group Art Unit
09/274,935	March 23, 1999	Alexander Markoff	1746

Invention: **COPPER CLEANING COMPOSITIONS, PROCESSES AND PRODUCTS DERIVED THEREFROM**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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cc:

#22

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

10/3

In re patent application of:	) Art Unit: 1746
K. Covert et al.	) Examiner: Alexander Markoff
Serial No.: 09/274,935	) Date: January 21, 2003
Filed: March 23, 1999	) Atty. Docket No.: EN997064
For: COPPER CLEANING COMPOSITIONS, PROCESSES AND PRODUCTS DERIVED THEREFROM	)

APPEAL BRIEF

Honorable Commissioner of Patents and Trademarks

Washington, DC 20231

S I R:

This Appeal is taken from the FINAL REJECTION of claims 1 through 20 as presented in the Office Action of December 4, 2001 (Paper No. 10), in the above-identified application.

REAL PARTY IN INTEREST

The real party in interest hereto is Appellants' assignee. The interest in the invention was assigned by the

inventors, to International Business Machines Corporation at the time of filing the application, and was recorded on Reel No. 010023, Frame No. 0741.

RELATED APPEALS AND INTERFERENCES

This appeal is the first appeal before the Office.

STATUS OF THE CLAIMS

All of the presently pending claims 1 through 20 now stand FINALLY REJECTED as of December 4, 2001 (Paper No. 10), which was reaffirmed in the Advisory Actions of March 29, 2002 (Paper No. 12), April 19, 2002 (Paper No. 15), and May 24, 2002 (Paper No. 18).

The rejection of claims 1 through 20 is hereby appealed.

STATUS OF THE AMENDMENTS

The subject patent application was filed on March 23, 1999. An Office Action rejecting claims 1 through 20 was mailed on December 21, 2000 (Paper No. 5). An Amendment and Affidavit were filed on April 4, 2002. An Office Action

again rejecting claims 1 through 20 was mailed on June 19, 2001. An Amendment was submitted on May 10, 2001. An Office Action finally rejecting claims 1 - 20 was mailed on December 4, 2001 (Paper No. 10). A Response after Final Office Action was filed on March 14, 2002. A first Advisory Action maintaining the rejection of claims was mailed on March 29, 2002 (Paper No. 12). A Response to the first Advisory Action was filed on April 11, 2002. A second Advisory Action maintaining rejection of the claims was mailed on April 19, 2002 (Paper No. 15). A Response to the second Advisory Action was filed on May 9, 2002. A third Office Action, maintaining rejection of the claims was mailed on May 24, 2002 (Paper No. 18). Applicants filed a Notice of Appeal on July 2, 2002.

SUMMARY OF THE INVENTION

The invention comprises microetching techniques for removing a small layer of copper from copper features forming part of a printed circuit board (page 2, paragraphs 1 and 2; and page 12, lines 1-4 of the specification). The etchants used are many which have been used before (page 5, lines 15-19), but the microetching techniques manage their use so that large quantities of copper are not removed (page 11, lines 3-12). The copper is selectively removed (page 12, lines 18-23) in the present invention by applying an inorganic acid

echant, persulfate and phosphate salts (page 11, lines 12-18). Microetching techniques are of recent vintage, and it is believed would not have been commonly used for fine line circuitry which came into vogue in the mid 1990's (page 8, paragraph 2).

ISSUES

Claims 1, 2, 5, 6, 8, 9 and 13 were finally rejected over the Japanese Reference No. JP 5-148,658, as anticipated under 35 U.S.C. §102(b). A first issue is whether the reference was applicable to microcircuitry. A second issue is whether the particulars of the claims, such as substrate materials and method steps, have been described by the reference. A third issue is whether the diametrically opposite purpose of the reference should qualify the reference as a valid teaching in the sense of 35 U.S.C. §§102 and 103. A fourth issue is whether the opposite teaching of nitric acid use in the reference is compatible with the teachings of the invention that eschews its use.

Claims 14 through 20 were finally rejected over the Japanese Reference No. JP 5-148,658, as unpatentable under 35 U.S.C. §103(a). Claims 3, 4, and 7 were finally rejected as unpatentable over the Japanese Reference No. JP 5-148,658, in view of U.S. Patent No. 4,238,279 (TSUBAI et al.) under 35

U.S.C. §103(a). The fifth issue is whether TSUBAI teaches or suggests the techniques presented in Appellants' specification. Claims 10 through 12 were finally rejected as unpatentable over the Japanese Reference No. JP 5-148,658, in view of U.S. Patent No. 5,855,805 (ARABINICK) under 35 U.S.C. §103(a). The sixth issue with respect to the ARABINICK reference is whether there is a teaching of the surfactants used by Appellant sufficient to make the combination rejection valid.

GROUPING OF THE CLAIMS

The claims cannot be grouped together, taking into account that claims 1 through 16 recite a microetching process for cleaning copper surfaces without removing bulk copper, and claims 17 through 20 recite methods of manufacturing intermediate circuit board structures.

ARGUMENT

The Honorable Board is respectfully requested to reverse the rejection of claims 1 through 20.

ISSUE No. 1

At the time of filing the above-identified application, microetching as a process for fine line circuitry was first coming into use in the industry, to the best of this Attorney's knowledge and belief.

ISSUE Nos. 1 and 2

This casts doubt on whether the main reference, JP 5-148,658, circa 1993, would even be relevant to the techniques being taught in the subject specification. In corroboration of this assumption is the admission by the Office in the FINAL REJECTION, (Office Action mailed December 4, 2001), page 3, line 7, wherein the cited Japanese reference "does not specify the specific substrates and conventional steps of the process of manufacturing of integrated circuits recited by the claims."

In the very description of this invention, Appellants state that despite using old substances for etching, the details of the technique prevent the bulk removal of copper common to non-microetching techniques. Therefore, with all due respect to the personnel of the USPTO, it is clear that the reference was probably not practicing microetching. This is particularly true by contrasting the large amount of method steps and detail in Appellants' specification. Can

claims 17 through 20 be rejected over JP 5-148,658 alone, on the basis of what is admitted to be a lack of detail of structure?

ISSUE No. 5

The much earlier reference to TSUBAI et al., circa 1980, used in combination to reject claims 3, 4, and 7, does not appear to comprise the microetching techniques called for by Appellants. Therefore, either alone or in combination, the purpose of the invention is not shown by the cited references

Irrespective of whether the Office makes that decision in Appellants' favor on that basis, however, it is questionable whether the rejection of claims 1, 2, 5, 6, 8, 9, and 13 as anticipated over the aforementioned JP 5-148,658 reference under 35 U.S.C. §102(b) is valid.

ISSUE No. 3

In the first instance, it is of significance that the purpose of the Japanese reference is almost diametrically opposite to those of Appellants' invention. Bulk copper removal is not the problem for this Japanese reference. The Japanese reference has a whisker forming problem, not a bulk copper removal problem. Appellants, on the other hand, are using much finer copper wire thicknesses. The Japanese

reference is being read into Appellants' invention, and it appears that where it coincides with similar chemistry, it fails by being an opposite teaching (i.e., the problem of growth of the copper (whiskers) versus Applicants' problem of bulk copper removal).

It appears that the Office has not addressed the above arguments with enough specificity throughout the prosecution. Rather, the prosecution seems to have focused on the fact of whether or not Appellants are teaching the use of nitric acid. Pages 3 and 4 of the specification specifically eschew the use of nitric acid as being too environmentally dangerous, and therefore should not be used in microetching; there is a problem of toxic byproducts. The Japanese reference uses nitric acid, as does TSUBAI et al.

ISSUE No. 4

On page 13, lines 9 through 11 appellants speak of nitric acid. The Office interprets this as contrary to Appellants' purposes. This is an obvious error because all through the specification, Appellants specifically refrain from its use. Even claim 5, which lists acid substances, does not recite nitric acid. Had Appellants wanted or intended to use nitric acid, they would have included it in claim 5. More importantly, however, Appellants believe that the statement on page 13, lines 9 through 11, does not actually suggest the

intended use of nitric acid. It is stated that it was "not preferred due to toxic byproducts such as nitrogen oxides." This is precisely in keeping with the statements on page 3 of the specification, and additionally as one of the advantages in paragraph (f) of the Summary of Invention, page 9 of the specification: "a stable, environmentally acceptable, and non-hazardous microetchant formulation."

The Office has inferred from that one sentence that the references that use nitric acid, viz., JP 5-148,658 and TSUBAI et al., are sufficient teachings of Appellants' invention. It is respectfully believed that this is a great leap of logic, particularly in view of the aforementioned Office admission that the Japanese reference does not teach the method steps, or structure of microelectronics.

ISSUE No. 6

The one cited reference that actually refers to microetchants is ARABINICK. The combination of ARABINICK with JP 5-148,658 to reject claims 10 through 12 does not teach the claimed invention, because ARABINICK does not teach the combination of etchant substances recited in claims 10 through 12. The Office admits in the Final Rejection (page 5, line 9) that the reference does not recite the specific surfactant claimed. The difference is not made up by the Japanese reference. The Office states, "the use of the

surfactants disclosed by ARABINICK in the method of JP5148658 for their primary purpose with reasonable expectation of adequate results because ARABINICK teaches that the use of these surfactants improves the process." This does not make sense, since the Office admitted just prior to this, that ARABINICK does not teach the surfactants of Appellants. In addition, the Office previously admitted that JP 5-148,658 did not teach the details of the invention.

Appellants respectfully believe that the rejections do not make sense, and that the cited references teach away from the invention, rather than towards the invention. More importantly, none of them, with the exception of ARABINICK, is particularly relevant.

Claims 14 through 20 were finally rejected over the Japanese Reference No. JP 5-148,658, as unpatentable under 35 U.S.C. §103(a). Appellants respectfully believe that the process steps described in claims 1 through 13 involve the general cleaning of copper surfaces, whereas the process steps of claims 14 through 16 are specifically directed to precious metal and nickel surfaces, thus constituting a different inventive problem of galvanic or accelerated etching not addressed by the reference. Claims 17 through 20 recite a process for manufacturing an intermediate structure having an embedded resistor in the printed wiring board, and such a process is once again not mentioned by the reference.

These claims have been lumped together in forming the rejection of 35 U.S.C. §103, but require separate consideration.

CONCLUSION

The Honorable Board is respectfully requested to reverse the rejection of claims 1 through 20, and allow the subject application to issue as a patent.

Respectfully submitted,

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on 1/22/03 (Date of Deposit)

Mark Levy, Reg. 29188
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1/22/03
Date

Appendix

1. A process for cleaning copper surfaces of copper objects, without etching bulk copper from said objects, comprising contacting said surfaces with an aqueous solution comprising an inorganic acid, a persulfate salt and a phosphate salt.

2. The process as recited in claim 1, wherein said objects are copper features on intermediary and final structures of a microelectronic package, said microelectronic package comprising a dielectric substrate having at least one lateral outermost surface to which said copper features are attached.

3. The process as recited in claim 1, wherein said phosphate salt is selected from the group consisting of orthophosphate, metaphosphate, hydrogenphosphate and dihydrogenphosphate salts.

4. The process as recited in claim 3, wherein the cation in said phosphate salt is selected from the group consisting of cations of: ammonium, potassium, sodium, lithium, and water soluble alkaline metal cations.

5. The process as recited in claim 1, wherein said inorganic acid is selected from the group consisting of sulfuric acid, phosphoric acid, metaphosphoric acid and pyrophosphoric acid.

6. The process as recited in claim 1, wherein the cation in said persulfate salt is selected from the group consisting of alkali metals, ammonium and water soluble alkaline metal cations.

7. The process as recited in claim 1, wherein said aqueous solution comprises approximately 25-100 gm/liter sodium persulfate, up to about 3 volume% phosphoric acid, and up to about 0.116 Molar sodium phosphate.

8. The process as recited in claim 1, wherein said aqueous solution further comprises a surfactant.

9. The process as recited in claim 8, wherein said surfactant is anionic.

10. The process as recited in claim 9, wherein said anionic surfactant is selected from the group of compounds consisting of aryl sulfonates, alkyl sulfonates, aryl sulfates, alkyl sulfates and phosphate esters.

11. The process as recited in claim 8, wherein said surfactant is nonionic.

12. The process as recited in claim 11, wherein said nonionic surfactant is selected from the group of compounds consisting of nonyl phenol ethoxylated with 3-30 moles of ethylene oxide, octyl phenol ethoxylated with 3-30 moles of ethylene oxide, block copolymers of ethylene oxide and propylene oxide, and alkyl polyoxyalkylene ethers.

13. The process as recited in claim 2, wherein said copper features, comprise at least one of the group consisting of plated through holes, contact fingers, tabs, connecting pads, and external and fine line circuitry.

14. The process as recited in claim 13, wherein said intermediary and final structures of said microelectronic package further comprise precious metal/nickel or phosphorous/nickel plated features, wherein said surfaces of unplated said copper features are proximate said precious metal/nickel or phosphorous/nickel plated features, wherein said copper surfaces are unaffected by galvanic or accelerated etching of bulk copper from said aqueous solution.

15. The process as recited in claim 14, wherein said precious metal is gold or palladium.

16. The process as recited in claim 2, wherein said intermediary and final structures of said microelectronic package comprise an embedded nickel resistor.

17. A process to manufacture an intermediate structure of an embedded resistor printed wiring board, comprising the steps of:

a) providing a printed wiring board internal core comprising a dielectric substrate having at least one outermost lateral surface, copper features, and at least one nickel or nickel alloy planar resistor formed on said at least one of said outermost lateral surfaces; and

b) applying a microetch solution comprising an inorganic acid, a persulfate salt and a phosphate salt, to clean exposed surfaces of said copper features, without adversely affecting the resistor values of said at least one nickel or nickel alloy planar resistor.

18. The process to manufacture an embedded resistor printed wiring board, as described in claim 17, wherein said first and second dielectric substrates are selected from the group consisting of epoxy resins, polyimides, polytetrafluoroethylene (TEFLON), cyanates, cyanate esters, BT epoxies, and IBM Driclad epoxy, either unreinforced or reinforced with glass.

19. A process to manufacture a planar resistor in an intermediate structure printed wiring board, comprising the steps of:

a) providing a printed wiring board internal core comprising a dielectric substrate having at least one lateral outer surface and first copper features affixed to said at least one of said lateral outer surfaces;

b) applying a microetch solution comprising an inorganic acid, a persulfate salt and a phosphate salt, to said first copper features in order to clean exposed surfaces of said first copper features;

c) enhancing bond strength to subsequently applied dielectric materials by forming copper oxide on uppermost and sidewall surfaces of said first copper features;

d) applying a dielectric material to the first dielectric substrate to exposed said lateral outer surfaces of said dielectric substrate and to said first copper features in order to generate a multilayer laminate;

e) fabricating and plating through-holes through said dielectric material;

f) forming second copper features and at least one planar nickel or nickel alloy resistor on an uppermost surface of said dielectric material, said second copper features and said planar resistor being electrically connected to said first copper features through said plated through-holes; and

g) applying a microetch solution comprising an inorganic acid, a persulfate salt and a phosphate salt to said second copper features in order to clean exposed surfaces of said second copper features without adversely affecting the resistor values of said at least one nickel or planar nickel alloy resistor.

20. A process of manufacturing intermediary structures of a microelectronic package, comprising the steps of:

a) providing a microelectronic package comprising a dielectric substrate, said dielectric substrate having an outermost lateral surface with at least one component selected from the group consisting of unplated copper features, precious metal plated copper features, and copper circuit lines attached thereto;

b) applying an aqueous microetchant solution comprising inorganic acid, persulfate salt and phosphate salt, to said microelectronic package in order to clean

said unplated copper features, without causing galvanic etching of bulk copper from said components;

c) applying and processing a soldermask material to uppermost surfaces of said components in order to expose said copper features, while protecting said copper circuit lines with unprocessed soldermask material;

d) reapplying said acqueous microetchant solution from step (b), to said copper features in order to clean in-process oxides and other contaminants without galvanic etching of bulk copper from said copper features; and

e) applying an organic solderability preservative to said exposed unplated copper features to fabricate sites for mounting pads.